FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: PF980092

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR): 09/869397

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FR99/03298	28 December 1999 (28.12.99)	28 December 1998 (28.12.98)

TITLE OF INVENTION

PROCESS FOR THE SIMULTANEOUS RECORDING AND READING OF A DIGITAL AUDIO AND VIDEO DATA STREAM, AND RECEIVER FOR IMPLEMENTING THE PROCESS

APPLICANT(S) FOR DO/EO/US

Claude Chapel, Serge Defrance and Christophe Vincent

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210). attached to Item 13
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98. with 2 references attached.
14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail 20. Return postcard receipt
20. ☒ Other items or information: **CERTIFICATE OF MAILING UNDER 37 CFR 1.10**

EL 682442661US — "Express Mail" mailing no.

June 28, 2001 — Date of Deposit

I hereby certify that this application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

ANELIA URBAN — Typed or printed name of person mailing application

Anelia Urban — Signature of person mailing application

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/869397		

21. The following fees are submitted:.	CALCULATIONS PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :	
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO $1000.00	
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO $860.00	
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $710.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) $690.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860.00
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	8 - 20 =	0	x $18.00	
Independent claims	2 - 3 =	0	x $80.00	
Multiple Dependent Claims (check if applicable).			☐	

TOTAL OF ABOVE CALCULATIONS =		860.00
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) (check if applicable).	☐	
SUBTOTAL =		860.00
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +		
TOTAL NATIONAL FEE =		$860.00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) (check if applicable).	☐	40.00
TOTAL FEES ENCLOSED =		$900.00
	Amount to be: refunded	$
	charged	$ 900.00

☐ A check in the amount of to cover the above fees is enclosed.

☒ Please charge my Deposit Account No. 07-0832 in the amount of $900.00 to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 07-0832 A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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Francis A. Davenport
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FRANCIS A. DAVENPORT
NAME

36,316
REGISTRATION NUMBER

JUNE 28, 2001
DATE

EXPRESS MAIL LABEL NO. EL682442661US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Claude Chapel et al.

Filed : December 28, 1999 - PCT National Phase of PCT/FR99/03298

For : PROCESS FOR THE SIMULTANEOUS RECORDING AND READING OF A DIGITAL AUDIO AND VIDEO DATA STREAM, AND RECEIVER FOR IMPLEMENTING THE PROCESS

PRELIMINARY AMENDMENT

Hon. Commissioner of Patents and Trademarks

Box PCT

Washington, D.C. 20231

Sir:

In the US national phase application of PCT/FR99/03298 please enter the following amendments.

IN THE TITLE:

PLEASE ENTER NEW TITLE

Please delete the title and insert the new title as published in the PCT International Application, --METHOD FOR SIMULTANEOUSLY RECORDING AND READING DIGITAL AUDIO AND VIDEO DATA FLOW AND RECEIVER USING SAME--

IN THE SPECIFICATION

Please amend the specification as follows:

Page 1, line 5, after the title, insert the following:

--This application claims the benefit under 35 U.S.C.

EXPRESS MAIL LABEL NO. EL682442661US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Claude Chapel et al.

Filed : December 28, 1999 - PCT National Phase of PCT/FR99/03298

For : PROCESS FOR THE SIMULTANEOUS RECORDING AND READING OF A DIGITAL AUDIO AND VIDEO DATA STREAM, AND RECEIVER FOR IMPLEMENTING THE PROCESS

PRELIMINARY AMENDMENT

Hon. Commissioner of Patents and Trademarks

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Sir:

In the US national phase application of PCT/FR99/03298 please enter the following amendments.

IN THE TITLE:

Please delete the title and insert the new title as published in the PCT International Application, --METHOD FOR SIMULTANEOUSLY RECORDING AND READING DIGITAL AUDIO AND VIDEO DATA FLOW AND RECEIVER USING SAME--

IN THE SPECIFICATION

Please amend the specification as follows:

Page 1, line 5, after the title, insert the following:

--This application claims the benefit under 35 U.S.C.

§ 365 of International Application PCT/FR99/03298 filed December 28, 1999, which claims the benefit of French Application No. 9816491, filed December 28, 1998.

BACKGROUND OF THE INVENTION

1. Field of the Invention--

Page 1, line 24, insert as heading: --SUMMARY OF THE INVENTION--

Page 2, line 33, insert as heading:,
--BRIEF DESCRIPTION OF THE DRAWING--

Page 3, line 19, insert as heading: --DETAILED DESCRIPTION--

IN THE CLAIMS:

Page 20, line 1 delete, "Claims" and replace with
--What is claimed is:--

Please amend the claims as follows (clean version):

1. (AMENDED) A process for recording a digital video and audio data stream wherein recording being carried out on a medium organized in the form of logic blocks in series and comprising a recording and reading head, said process comprises the steps of:

recording data in one block out of two starting from a first block,

following the triggering of the reading of the data, alternately of reading a previously recorded block and of continuing the recording in the block following the block read.

2. (AMENDED) The process as claimed in claim 1, wherein when the set of blocks recorded before the triggering of reading have been read, recording is continued in contiguous blocks in a non-interlaced manner.

3. (AMENDED) The process as claimed in claim 1, wherein when the set of blocks recorded before the triggering of reading have been read, recording is continued in a loop in the blocks previously read.

4. (AMENDED) The process as claimed in claim 1, wherein when the set of blocks recorded before the triggering of reading have been read, said blocks are read, then rewritten in a non-interlaced manner.

5. (AMENDED) The process as claimed in claim 1, wherein the recording of data is performed in a group of N contiguous blocks ($N > 1$) out of two instead of a single block out of two.

6. (AMENDED) The process as claimed in claim 1, comprising an additional step of, detecting sequences of free blocks on the medium and of applying steps of recording and of reading inside such sequences.

7. (AMENDED) A digital television receiver comprising means for receiving a digital audio and video data stream, comprising:

a recording medium furnished with a recording and reading head, said medium being organized in the form of logic blocks in series;

a control circuit for managing the writing and the reading of blocks of the recording medium;

an interfacing circuit for interfacing the recording medium with said control circuit, said control circuit initially instructing the recording of data in one block out of two starting from a first block and subsequently, following the triggering of the reading of the data, alternately the reading of a block previously recorded and the continuing of the recording in the block following a block read.

8. (AMENDED) The receiver as claimed in claim 6, wherein the control circuit instructs the recording of data in a group of N contiguous blocks ($N > 1$) out of two instead of a single block out of two.

IN THE ABSTRACT:

Page 22 delete Abstract and replace with a substitute Abstract supplied herewith on a separate sheet.

REMARKS

The specification has been amended to include a reference to the priority applications. The claims are amended to eliminate multiple dependencies, reference indicia and to meet the requirements of the USPTO. A marked up version of the claims is supplied on a separate sheet. A replacement Abstract is supplied on a separate sheet.

No fee is believed to have been incurred by virtue of this amendment. However if a fee is incurred on the basis of this amendment, please charge such fee against deposit account 07-0832.

Respectfully submitted,

Claude Chapel et al.

By:- Francis A. Davenport

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Registration No. 36,316
609-734-9864

THOMSON multimedia Licensing Inc.
Patent Operation
PO Box 5312
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June 28, 2001

Marked Up Claims

1. (AMENDED) A process for recording a digital video and audio data stream [characterized in that] wherein recording being carried out on a medium [(201)] organized in the form of logic blocks in series and comprising a recording and reading head, said process comprises the steps of:

[of] recording data in one block out of two starting from a first block,

following the triggering of the reading of the data, alternately of reading a previously recorded block and of continuing the recording in the block following the block read.

2. (AMENDED) The process as claimed in claim 1, [characterized in that] wherein when the set of blocks recorded before the triggering of reading have been read, recording is continued in contiguous blocks in a non-interlaced manner.

3. (AMENDED) The process as claimed in claim 1, [characterized in that] wherein when the set of blocks recorded before the triggering of reading have been read, recording is continued in a loop in the blocks previously read.

4. (AMENDED) The process as claimed in [one of claims 1 or 2] claim 1, [characterized in that] wherein, when the set of blocks recorded before the triggering of reading have been read, said blocks are read, then rewritten in a non-interlaced manner.

5. (AMENDED) The process as claimed in [one of the preceding claims] claim 1, [characterized in that] wherein the recording of data is performed in a group of N contiguous blocks (N > 1) out of two instead of a single block out of two.

6. (AMENDED) The process as claimed in [one of the preceding claims] claim 1, [characterized in that it furthermore comprises the] comprising an additional

step of, detecting sequences of free blocks on the medium and of applying steps of recording and of reading inside such sequences.

7. (AMENDED) A digital television receiver comprising means [(101)] for receiving a digital audio and video data stream, [characterized in that it comprises] comprising:

- a recording medium [(201)] furnished with a recording and reading head, said medium being organized in the form of logic blocks in series;
- a control circuit [(107)] for managing the writing and the reading of blocks of the recording medium [(201)];
- an interfacing circuit [(202 to 214)] for interfacing the recording medium with said control circuit [(107)], said control circuit initially instructing the recording of data in one block out of two starting from a first block and subsequently, following the triggering of the reading of the data, alternately the reading of a block previously recorded and the continuing of the recording in the block following a block read.

8. (AMENDED) The receiver as claimed in claim 6, [characterized in that] wherein the control circuit instructs the recording of data in a group of N contiguous blocks (N > 1) out of two instead of a single block out of two.

ABSTRACT

A method for recording a digital video and audio data stream where the recording is performed on a medium organized in the form of logic blocks in series and comprising a recording and reading head. The method comprises the steps of recording data in one block out of two starting from a first block; following the triggering of data reading, alternately reading a previously recorded block while proceeding with the recording while proceeding with the recording in the block coming after the read block. The invention also concerns a digital television receiver set using said method.

Process for the simultaneous recording and reading of a digital audio and video data stream, and receiver for implementing the process

The invention relates to a process for the simultaneous recording and reading of an audio and video data stream, in particular of data compressed according to the MPEG II standard, on a recording medium furnished with a reading and recording head. The invention also relates to a digital television receiver implementing the process.

When one wishes to record sequential data on a medium furnished with a head responsible both for the reading and recording of the data, the time required for this head to make a jump from one recording logic unit (block) of the medium to another unit might not be negligible. The time of movement of a head of a commercially available hard disk may for example be of the order of 10 to 12 ms. In particular in the case of the recording of compressed audio and video data requiring a minimum throughput, it may be necessary to limit the number of jumps made by a head so as to avoid the drying up of the buffer memory used for decoding this data.

The inventors have in particular observed that this problem could become manifest if one wishes to read a data stream in non-real-time, whilst the recording of this stream is continued during the reading of the data previously recorded.

The purpose of the invention is to propose a recording process which avoids unnecessary jumps of the reading and recording head.

The subject of the invention is a process for recording a digital video and audio data stream characterized in that, recording being carried out on a medium organized in the form of logic blocks in series and comprising a recording and reading head, said process comprises the steps:

- of recording data in one block out of two starting from a first block,
- following the triggering of the reading of the data, alternately of reading a previously recorded block and of continuing the recording in the block following the block read.

During writing without reading, a single jump of the head is performed. During reading while continuing recording, no jump is

performed: the reading head reads a block and records in the immediately following block. Thus, the number of jumps is reduced effectively.

According to a particular embodiment, when the set of blocks recorded before the triggering of reading have been read, recording is continued in contiguous blocks in a non-interlaced manner.

According to a particular embodiment, when the set of blocks recorded before the triggering of reading have been read, recording is continued in a loop in the blocks previously read.

According to a particular embodiment, the recording of data is performed in a group of N contiguous blocks (N > 1) out of two instead of a single block out of two.

According to a particular embodiment, said process furthermore comprises the additional step of detecting sequences of free blocks on the medium and of applying steps of recording and of reading inside such sequences.

The subject of the invention is also a digital television receiver comprising means for receiving a digital audio and video data stream, characterized in that it comprises:

- a recording medium furnished with a recording and reading head, said medium being organized in the form of logic blocks in series;
- a control circuit for managing the writing and the reading of blocks of the recording medium;
- an interfacing circuit for interfacing the recording medium with said control circuit, said control circuit initially instructing the recording of data in one block out of two starting from a first block and subsequently, following the triggering of the reading of the data, alternately the reading of a block previously recorded and the continuing of the recording in the block following a block read.

According to a particular embodiment, the control circuit instructs the recording of data in a group of N contiguous blocks (N > 1) out of two instead of a single block out of two.

Other characteristics and advantages of the invention will become apparent through the description of a particular nonlimiting exemplary embodiment illustrated by the appended figures among which:

- figure 1 is a block diagram of a digital receiver/decoder comprising a storage device in accordance with the present exemplary embodiment;

- figure 2 is a block diagram of an exemplary embodiment of the storage device, in this instance a hard disk;
- figure 3 is a diagram illustrating the split of audio and video areas in a FIFO-type memory used as buffer for the writing of data;
- figure 4 is a diagram of a block of 128 Kbytes of a part of the hard disk that is reserved for the recording of audio and video streams;
- figure 5 is a diagram illustrating the two types of file system present on the hard disk;
- figure 6 is a diagram illustrating various areas for recording the 'stream'-type file system;
- figure 7 is a flow chart for the writing of a file to the disk;
- figure 8 is a diagram illustrating the respective durations of various operations during a reading of blocks;
- figures 9a and 9b are diagrams illustrating a process making it possible to reduce the movements of a disk writing/reading head when recording and reading simultaneously;
- figure 10 is a block diagram of a clock recovery circuit.

Although the description hereinbelow relates especially to the recording of demultiplexed audio and video PES packets, the invention can easily be applied to the direct recording of transport stream (TS) or program (PS) packets or else of other types of steams, for example of Digital Video (DV) type.

According to the present exemplary embodiment, the storage device is a hard disk built into a digital television decoder meeting the DVB standard.

Figure 1 is a block diagram of such a decoder. The latter comprises a tuner 101 linked to a demodulation and error correction circuit 102 which also comprises an analog/digital converter for digitizing the signals originating from the tuner. Depending on the type of reception, cable or satellite, the modulation used is of QAM or QPSK type, and the circuit 102 comprises the demodulation means appropriate for the type of reception. The demodulated and corrected data are serialized by a converter 103, connected to a serial input of a demultiplexing and decoding circuit 104.

According to the present example, this circuit 104 is an STi5500 circuit manufactured by ST Microelectronics. The latter comprises, linked to a central 32-bit parallel bus 105, a DVB demultiplexer 106, a

microprocessor 107, a cache memory 108, an external memory interface 109, a serial communication interface 110, a parallel input/output interface 111, a chip card interface 112, an audio and video MPEG decoder 113, a PAL and RGB encoder 114 and a character generator 115.

The external memory interface 109 is linked to a 16-bit parallel bus to which are respectively linked a parallel interface 116 of IEEE 1284 type, a random access memory 117, a "Flash" memory 118 and a hard disk 119. The latter is of EIDE type for the requirements of the present example. The parallel interface 116 is also connected to an external connector 120 and to a modem 121, the latter being linked to an external connector 122.

The serial communication interface 110 is linked to an external connector 123, as well as to the output of an infrared reception subassembly 124 intended to receive signals from a remote control (not illustrated). The infrared reception subassembly is integrated into a front panel of the decoder, which also comprises a display device and control buttons.

The chip card interface 112 is linked to a chip card connector 125.

The audio and video decoder 113 is linked to a 16-Mbit random access memory 126 intended for storing the nondecoded audio and video packets. The decoder transmits the decoded video data to the PAL and RGB encoder 114 and the decoded audio data to a digital/analog converter 127. The encoder supplies the RGB signals to an SECAM encoder 132, and also provides a video signal in the form of a luminance component Y and of a chrominance component C, these two components being separated. These various signals are multiplexed through a switching circuit 128 to an audio output 129, television output 130 and video recorder output 131.

The route taken by the audio and video data through the decoder is as follows: the demodulated datastream possesses a transport stream format or more simply a "TS" format with reference to the MPEG II Systems standard. This standard possesses the reference ISO/IEC 13818-1. In their header, the TS packets comprise identifiers called PIDs which indicate the elementary stream to which the useful data of the packet pertain. Typically, an elementary stream is a video stream associated with a particular program, whereas an audio stream of this program is another one. The data structure used to transport the

compressed audio and video data is referred to as an elementary stream packet or else "PES" packet.

The demultiplexer 106 is programmed by the microprocessor 107 so as to extract from the transport stream the packets corresponding to certain values of PID. The useful data of a demultiplexed packet are, as appropriate, descrambled (if the rights stored by a chip card of the user authorize this descrambling), before storing these data in buffer areas of the various memories of the decoder. The buffer areas reserved for the audio and video PES packets are situated in the memory 126. The decoder 113 reads back these audio and video data depending on its needs, and transmits the decompressed audio and video samples to the encoder 114 and to the converter 127 respectively.

Certain of the circuits mentioned above are controlled in a known manner, for example through a bus of I2C type.

The typical case described hereinabove corresponds to the direct decoding of a demultiplexed program by the MPEG decoder 113.

According to the invention, the receiver/ decoder comprises a hard disk for the mass storage mainly of audio and video data in their compressed form.

Figure 2 is a block diagram of the assembly 119 comprising the hard disk and the interfacing circuits linking it to the external memory interface 109.

The hard disk 201 is a commercial hard disk furnished with an Ultra ATA/EIDE interface. 'ATA' designates the communication protocol, known elsewhere, of the specific disk used within the framework of the present example. According to the present exemplary embodiment, the disk comprises a double file system. Two file systems; associated with respective data areas are used in parallel to read and write data from and to the disk, the first file system being adapted to the writing and to the reading of data of computer file, program, code type, etc. referred to hereinbelow as the 'block' file system, whilst the second file system is intended for the writing and for the reading of audio and video streams, this file system being referred to hereinbelow as the 'stream' file system.

This duality is also found at the level of the architecture of the interface circuits of figure 2.

The writing and reading of data blocks are performed by way of respectively a memory of first-in-first-out (FIFO) type 202 for writing and of a memory 203 of the same type for reading. The two FIFO memories have

a respective size of 16 bytes and are controlled by a block transfer circuit 204 which manages the address pointers for these two FIFO memories. According to the present exemplary embodiment, these are double synchronous port type memories.

The data exchanges according to the 'block' mode are carried out in direct memory access mode, by sending bursts of 16 bytes. These bursts are buffered both in write mode and in read mode by the two FIFO memories 202 and 203, which allow the adaptation of the disk bit rate to the bus bit rate 215 and vice versa.

Two FIFO memories 205 and 206 are provided for respectively writing and reading the audio and video streams. Each FIFO memory 205 and 206 comprises, according to the present exemplary embodiment, a physical memory of 512 Kbytes, divided up into four video banks of 112 Kbytes (clustered into a 'video' area, referenced 205a, respectively 206a) and an audio area of 64 Kbytes (referenced 205b, respectively 206b), and is controlled by a stream transfer control circuit 207. Each video bank and audio area is managed as a first-in-first-out (FIFO) memory. The circuit 207 manages two write pointers and two read pointers which are independent for each of the series 205 and 206, namely a pair of video pointers and a pair of audio pointers. A single memory 205 and 206 is active in read mode and a single is active in write mode at a given moment. Access to the two memories 205 and 206 is however independent, allowing so-called simultaneous reading and writing from and to the disk.

According to a variant of the present exemplary embodiment, the memories 202, 203, 205 and 206 are areas of the random access memory 117, each of these areas being managed as one, or if appropriate several, memory (memories) of the first-in-first-out type.

Moreover, an adaptation of the present exemplary embodiment to the management of additional components, such as for example several elementary audio streams, would be easily achievable by the person skilled in the art, by providing the additional memories required for this purpose.

Moreover, it is also possible to record TS stream packets directly, without having to extract the PES packets therefrom. In this case, the nature (audio, video or other) of the content of the packets recorded is of no concern and the demultiplexed TS packets are recorded in blocks of 128 Kb, that is to say by continuously managing the 112 and the 16 Kb. In this particular case, therefore, there is no reframing depending on the

nature of the elementary packets contained in the TS packets, unlike what is done when recording the PES packets rid of the transport layer.

The two transfer control circuits 204 and 207 are state machines whose operation is controlled by the microprocessor 107. The microprocessor tells the controllers the transfer tasks to be performed in direct memory access mode (the mode referred to hereinafter as the 'UDMA' or Ultra Direct Memory Access mode), and is forewarned of the accomplishing of these tasks through an interrupt generated by an interrupt control circuit 208 linked to the two transfer control circuits 204 and 207. Within the framework of the example described here, use is made of the 33 Mbyte/s UDMA mode, but the invention is obviously not limited to this mode.

The two transfer control circuits manage disk access proper through a control circuit 209 which allows implementation of the disk and its mode of access, namely access to the command and control registers and direct UDMA memory access. The command circuit is also linked to the microprocessor 107, for the direct management of the control and command registers of the disk, this not implementing the transfer control circuits 204 and 207.

The interfacing circuit of figure 2 furthermore comprises two multiplexers 210 and 211, which receive as input respectively the three input paths for the data, that is to say the data to be written to the disk, and the three output paths for the data, that is to say for the data read from the disk. Each multiplexer therefore possesses at input three 16-bit buses and one 16-bit bus at output. The switching between the various paths is managed by the microprocessor 107.

As far as the writing multiplexer 210 is concerned, the first input path consists of a direct access of the data bus 215 of the external memory interface 109 to the data bus 212 of the disk 201, the second path consists of the output of the FIFO memory 202 for the writing of blocks, whilst the third path consists of the output of the FIFO memory 205, for the writing of the streams.

As far as the reading multiplexer 211 is concerned, the first output path consists of a direct access of the data bus of the disk to the data bus of the external memory interface 109, whilst the second path consists of the output of the memory 203 for the reading of blocks, and the third path of the output of the FIFO memory 206, for the reading of streams.

The respective outputs of the two multiplexers 210 and 211 are connected respectively to the data bus of the disk and to the data bus of the external memory interface across three-state output stages 213 and 214, controlled by the automata 204 and 207.

Each memory 205 and 206 serves as cache memory for the data heading for the disk or coming from it. The disk according to the present exemplary embodiment comprises sectors of 512 bytes. The content of 256 sectors therefore corresponds to the size of a video memory bank of a FIFO memory of one of the memories 205a and 206a, plus a quarter of the size of one of the audio areas 205b and 206b, namely a total of 128 Kbytes. This is substantially the quantity of data transferable from or to the disk during the mean time of movement of a reading head of the disk used in the present example, namely around 10 ms.

The use of FIFO memories having the characteristics defined hereinabove has made it possible to obtain simultaneous reading and writing bit rates of 15 Mbit/s.

The writing of an audio/video stream to the disk will be described in conjunction with figures 3 and 4.

Figure 3 illustrates the splitting of the PES format audio and video data in accordance with the MPEG II standard to two FIFO memories, namely a video bank (one of the banks of the part 205a of the memory 205) and an audio area (part 205b of the memory 205).

The data are written to the disk in audio/video blocks of 128 Kbytes each. According to the present invention, a fixed part of the block of 128 Kbytes is reserved for video data (112 Kbytes) and another part, which is variable, for the audio data (16 Kbytes maximum). The blocks being written sequentially, the audio and video data are therefore interleaved on the disk.

It has been found that the ratio of the minimum bit rate of a video stream to the maximum bit rate of an audio stream is around 10. By defining in a block of 128 Kbytes an area of 112 Kbytes reserved for video and of 16 Kbytes for audio, the ratio is 7. Stated otherwise, by taking into consideration an audio/video stream whose video data (in the form of video PES packets) are stored as soon as they are multiplexed in the area of 112 Kbytes and whose audio data (in the form of audio PES packets) in the area of 16 Kbytes, the video area will always be filled before the audio area.

It is obvious that, depending on the streams and the bit rates to be managed, ratios other than 7 may also be used. This is the case in particular if compression algorithms other than those advocated by the MPEG standard are implemented.

When the video bank of 112 Kbytes is filled, the content of this bank is written to the disk, followed by the audio data accumulated during the same time as the 112 Kbytes of video data, this being irrespective of the state of fill of the audio area. By construction, one nevertheless knows that fewer than 16 Kbytes have been accumulated.

In this context, there is no correlation between the limits of the PES packets and the start or the end of a video bank or of the audio data accumulated. The first data of the content of a video bank may in fact fall in the middle of a video PES packet, whilst the last audio data items accumulated do not necessarily correspond to the end of an audio PES packet.

It will be assumed that the measures required for opening a file for writing a stream have been taken beforehand at the disk file system level.

Appended to the video and audio data are an identifier of the file to which the block of the disk belongs and a data item indicating the quantity of audio data, which is derived from the state of the write pointer of the audio area 205b of the memory 205 at the time the limit of fill of the video bank is reached. The identifier is coded on 16 bits, whilst the quantity of audio data is coded on 14 bits. Figure 4 illustrates the layout of the data in a block on the disk. Part of the audio area of the block not containing any audio data is filled with stuffing bits so as to make these data up to 16 Kbytes.

In the case of the recording of TS packets, it is obviously not necessary to indicate a quantity of audio data.

The file identifier is the same for all the blocks belonging to the same file. The identifier of a file is information which is redundant to that contained in a data structure referred to as a node and associated with each file. The identifier is however used if a write-open file has not been correctly closed: the file system then identifies all the blocks belonging to one and the same file by virtue of the file identifier and updates the corresponding parameters in the node of the file and in the other data structures recorded at the start of the part of the disk reserved for the 'stream' file system. The receiver knows the identifier of the open file since

the latter is written in a flag on the disk (at node number 0) at the start of each file opening, this flag being reset to zero upon the closure of this file.

It is apparent that the aligning of the audio data with the video data brings about the nonuse of a variable part of the 16-Kbyte audio area of a block of the disk. However, the size of this unused part is relatively small compared with the 128 Kbytes of the complete block. If the recording of the video and audio packets were performed in the order of demultiplexing of the PES packets, then the recording of the nature of each packet (audio or video, for example in the form of a PID identifier) would have been necessary. The room required for this recording would have been on the one hand greater than that reserved for the stuffing bits in the audio part of the recorded blocks and on the other hand more complex to manage.

The advantages of aligning the audio data with the video data are however considerable. Specifically, even if the audio and video data are not multiplexed in the same way as in the incoming audio/video stream, the synchronism between audio and video data is maintained overall. The audio data in a block are in fact those having been received temporally multiplexed with the video data of the same block. It is thus possible to restore an audio/video stream at the decoder without any drift in synchronism which could cause overflow of audio or video buffers during read back.

Synchronism is also maintained if the TS stream is recorded directly.

The use of four video memory banks of 112 Kbytes each in read and/or write mode, as well as of an audio area of 64 Kbytes, makes it possible to compensate for the disk write head movement times and for any disk access problems which could delay writing. The microprocessor 107 nevertheless attempts to keep the largest number of banks of the memory 205 empty, and this may be referred to as management of empty buffer type. To transfer the audio/video data to the disk, the microprocessor 107 triggers a direct memory access mechanism ('DMA') which performs the transfer of the audio/video data from the demultiplexer 106 to a video bank and the audio area of the FIFO memory 205. Within the framework of the exemplary embodiment, this is a DMA built directly into the demultiplexer 106.

When a video bank of the memory 205 is full, the write transfer control circuit 207 generates an interrupt destined for the microprocessor

107, writing being continued in the next video FIFO memory bank. The video FIFO memory banks are implemented in rotation. The microprocessor, which also manages the disk file system, determines the first write sector of 512 bytes of the block of 128 Kbytes, and supplies it to the disk by way of the control circuit 209. The microprocessor also initializes the direct memory access mechanism at the disk for the transfer of data from the first video FIFO memory bank and the corresponding quantity of audio from the audio FIFO 205b of the memory 205. The disk then writes 128 Kbytes to 256 sectors under control of the circuit 207. After transferring the 128 Kbytes of data, the hard disk exits the Ultra DMA mode, the control circuit 207 frees the Ultra DMA mode and tells the microprocessor through an interrupt. This transfer is repeated each time the microprocessor receives an interrupt request by way of the control circuit 207 and until there is a decision to stop the recording. The microprocessor then updates the node corresponding to the file in which writing took place, as well as the corresponding bit tables. The role of the bit tables and of the node will be seen in greater detail hereinbelow.

It should be noted that, according to the present exemplary embodiment, the audio area of each memory 205 and 206 is not organized as banks of fixed size, as is the case for the video banks of 112 Kbytes. The audio areas are managed by storing, in write mode, the quantity of audio data written for each associated video bank and, in read mode, by taking into account the information relating to the audio quantity read from each block.

According to the present exemplary embodiment, only the PES data are recorded on the disk. This implies that the reference clock values ('PCR') are not recorded. However, as already mentioned, it would also be conceivable to record packets of the TS transport layer.

The reading mechanism differs substantially from the writing mechanism. We consider a reading initialization phase and a steady reading condition.

To initialize reading in stream mode, the microprocessor sends the hard disk the address of the first sector of the first block to be transferred and requests the transfer of 256 sectors. Once the transfer is completed, the transfer control circuit 207 generates an interrupt to indicate the end of the transfer. The microprocessor then requests the transfer of the next block, and so on and so forth until four video FIFO memory banks of the block 206 (and a part of the audio area 206b) are

filled. The transfer and the decoding of data to the decoder 113 are initialized only then by the microprocessor. Once initialization has been performed, the data are transferred without the intervention of the microprocessor: the decoder 113 reads the audio and video data as and when the requirements alter. The speed with which the FIFO memories are emptied depends in fact on the content of the compressed audio and video packets.

The steady condition is as follows: when a memory bank of 112 Kbytes of video FIFO is completely emptied (and the corresponding audio data have also been read), an interrupt request will notify the microprocessor thereof, and the latter triggers the transfer of a new block, in such a way as if possible to keep all the FIFO video banks full. This management is of the full buffer type.

According to the present exemplary embodiment, the recovery of the system clock is performed by demultiplexing transport packets corresponding to a program in progress, and by locking a phase-locked loop to the reference clock values ('PCR') of an incoming TS stream. This operation makes it possible to obtain the required clock frequency of 27 MHz. Hence, an incoming TS stream is used to recover the reference clock rate, even if this clock is used in conjunction with audio and video data which are not broadcast in real time in this stream.

This principle of clock rate recovery is illustrated by the block diagram of figure 10, which comprises a phase-locked loop (PLL) composed of a comparator/subtracter 1001, followed by a low-pass filter 1002 and by a voltage-controlled oscillator 1003. A counter 1004 closes the loop between the output of the oscillator 1003 and an input of the comparator/ subtracter 1001. The comparator/subtracter furthermore receives the PCR clock values emanating from a TS stream. The difference between a local clock value emanating from the counter 1004 and the PCR clock value is sent to the low-pass filter 1002, and the rate of the loop output signal is adapted accordingly. The clock value contained in the counter 1004 is regularly updated with the demultiplexed PCR clock value, this having the effect of synchronizing the counter 1004 with the clock of the encoder of the TS stream. This clock is used for the decoding and presentation of the TS stream received in real time. As described hereinbelow, only the clock rate at the output of the PLL loop is used for the decoding and presentation of data read from the hard disk.

Other clock recovery processes can be employed. It is in particular possible to use a free clock. Specifically, the accuracy required for the 27-MHz clock is not necessarily as high as that imposed by the MPEG II standard at the level of the encoder, namely 30 ppm. This accuracy is actually required only if a stream originating directly from an encoder needs to be decoded. In fact, in such a case, excessive drifting of the clock of the decoder can cause the buffer memory of the decoder to dry up or overflow. However, in the case of the reading of a stream from a local hard disk, the inventors have found that this constraint disappears: the decoder can in fact regulate the bit rate of the stream in read mode as a function of its requirements, this not being the case when the stream reaches it directly, without it having passed through the buffer constituted by the disk.

The decoding of the video frames is triggered at a given level of fill of a decoding buffer, forming part of the random access memory 126. This level is for example 1.5 Mbit for a buffer with a capacity of 1.8 Mbit. This instant, called top buffer video, is regarded as reference instant for the decoding and presentation of the video frames. The DTS clock value of the first frame read from the buffer of the decoder is loaded into the counter 1005 of figure 10. This counter counts at the clock rate generated by the PLL loop. Decoding of the first video frame is triggered immediately, whilst the presentation of this first frame and the decoding and presentation of the following frames is performed according to the corresponding DTS and PTS clock values, relative to the clock generated by the counter 1005.

The decoding and presentation of the audio frames also call upon the clock thus regenerated.

Figure 5 illustrates the way in which the two file systems 'block' and 'stream' share the use of the hard disk. According to the present exemplary embodiment, the 'block' file system and its associated data area occupy several hundred megabytes, whilst the 'stream' file system and its data area occupy several gigabytes.

The 'block' file system will not be detailed further, the organization of the corresponding file system being devised in a conventional manner, of the UNIX or MINIX type for example, comprising a 'super block', a table of nodes, a table of data blocks, as well as the node and data areas proper. A characteristic of this file system is however that it favors random access to the data, for example through the use of multiple indirect addressing (that is to say a series of address pointers only the last

of which gives the address of the sought-after data block), whilst the 'stream' file system has the characteristic of optimizing sequential access.

The hard disk furthermore comprises a single boot block for both the two file systems. The parameters appearing in the boot block are the index of the boot program, the name of the volume, the number of bytes per sector, the number of sectors of the volume, and the number of sectors of the boot block.

As already mentioned, the parameters chosen for the 'stream' file system are the following: the size of a sector is 512 bytes, a 'stream' block comprising 256 sectors.

This is to be compared with the size of a block of the 'block' file system, namely 4 sectors.

Figure 6 illustrates the organization of the 'stream' file system. This file system comprises firstly a block referred to as a 'superblock', containing general information about the file system. Table 1 gives the information contained in this superblock:

8-Bit file identifier
Name of the volume
Date of creation of the volume
Date of the last modification
Total size of the part of the disk allocated to the 'stream' file system and to its data blocks (in sectors)
Size of the superblock (in sectors)
Address of the superblock
Address of the copies of the system files (1st copy)
Address of the copies of the system files (2nd copy)
Address of the copies of the system files (3rd copy)
Address of the copies of the system files (4th copy)
Size of the nodes (in sectors)
Address of the first node
Size of the sequence file area (in sectors)
Address of the sequence file area
Size of the bit tables (in sectors)
Address of the table of bits of the nodes
Address of the table of bits of the sequence files
Address of the table of bits of the blocks of data
Maximum number of files (also maximum number of nodes)
Maximum number of sequence files
Number of sectors per block of data
Address of the first data item (number of the first block)

Table 1

The addresses are given in terms of sector numbers, all the sectors of the disk being numbered from 0 up to the maximum number of sectors of the disk.

Associated with each file or directory of the file system is a data structure referred to as a 'node' which indicates the name of the file or of the directory, its size, its location and that of its attributes. The nodes are grouped together in the file system after the superblock. Table 2 indicates the composition of a node:

Name of the file or of the directory
Identifier of the file or of the directory (on 32 bits)
Size (in bytes)
Identifier of the parent directory (on 32 bits)
Pointer to the attributes
For a file: list of a maximum of 15 sequences of contiguous blocks defining the file For a directory: list of identifiers of the files or subdirectories contained in this directory
Pointer to an extension of the previous field (for example a sequence file identifier in the corresponding area)

Table 2

A sequence is a run of contiguous blocks forming part of one and the same file. It is defined by the address of the first block of the sequence, followed by the number of contiguous blocks. If the file is fragmented, a pointer returns to an extension area comprising additional sequences (area of sequence files) with the aid of an appropriate file identifier. In turn, a sequence file can return to an additional file, and so on and so forth. This type of simple indirect addressing is well suited to the sequential nature of the data. This avoids successive manipulation with several pointers, such manipulation being expensive in terms of time. The multiple indirect addressings are reserved for the 'block' file system, with a view to facilitating random access to the data.

The attributes are stored in the 'blocks' file system. It is therefore possible to make reference from one file system to data managed in the other.

The additional sequence files are grouped together in the 'sequences' section after the area reserved for the nodes (see Figure 6).

The 'stream' file system furthermore comprises a 'bit table' indicating for each node, each additional sequence file and each block of data whether or not it is occupied. To this end, a bit is associated with each node, additional sequence file and block.

Figure 7 is a flow chart of the process for writing a file. Initially, a node associated with the file is created. A locating of this node on the disk is determined by scanning the table of bits of the nodes. By using the table of bits of the blocks, the microprocessor 107 determines a free sequence

of blocks and writes the data to be recorded to it, block after block. At the end of the sequence, the address and the length of the sequence are stored in the node of the file in memory. The flags of the table of bits of the blocks corresponding to the blocks allocated to the recording of the sequence are then updated in a table in memory. The operation of detecting and writing a sequence is repeated if necessary, until the complete file has been recorded. Once the recording of the data is completed, the updated information relating to the location of the data (that is to say the node and the bit tables updated) are themselves recorded on the disk. The information is written to the disk only at the end of recording, so as to avoid incessant toings and froings by the read/write head.

To read a file, the microprocessor firstly reads the node of this file, as well as the definitions of all the additional sequences referring thereto. This avoids movement of the disk read/write head during reading to the areas at the start of the file system.

One of the envisaged applications of the disk is the non-real-time reading of a program currently being recorded. For example, the television viewer watching a live program has to go away for a few minutes and wishes to resume watching at the exact moment at which this was interrupted. When he goes away, he starts the recording of the program. On his return, he triggers the reading of the program, although the recording of the latter is still in progress. Given that the read/write head must perform movements from the reading areas to the writing areas and vice versa and that the time of movement of the head is of the order of 10 ms for the disk used within the framework of the present example, certain precautions have to be taken to guarantee the minimum bit rate required for reading and writing.

To assess the influence of head jumps on bit rate, we consider the least favorable conditions by taking the example of the maximum bit rate of an MPEG II stream, namely 15 Mbit/s, a block of 128 Kbytes thus corresponding to 66.7 ms of audio and video data, as illustrated by figure 8. The reading or writing of a block, at a transfer rate of 96 Mbit/s, lasts 10.4 ms. If reading is not preceded by a jump, 56.3 ms remain available as a safety margin.

As indicated in the previous paragraph, a head jump from a first block to a second block which is not adjacent to the first block takes 10 ms. Hence, a free interval of 46.3 ms remains.

If a read and a write each preceded by a jump are to be performed within an interval of 66.7 ms, only 25.9 ms remain available. Since defective sectors within a block may also give rise to jumps of the head, it is preferable to limit the number of jumps in read mode and write mode to the minimum.

According to the present exemplary embodiment, the number of head jumps during simultaneous recording and reading is reduced by effecting interleaved writing of the blocks, as illustrated by figures 9a and 9b.

When the recording of the program is triggered (for example by the television viewer), writing is performed every other block in a sequence of adjacent blocks. This is illustrated by figure 9a. A jump of the read head is therefore performed before writing each block.

When the reading of the program is triggered, writing is continued in the blocks left free previously. For example, following the reading of the first block written (the one furthest to the left in figure 9b), the next write is performed in the immediately adjacent block. No jump of the read/write head is then performed between reading in the first block and writing in the second block. The reduction in the number of jumps of the head also results in a consequent reduction in the noise generated by these movements.

Once all the blocks written before the start of reading have been read out, writing is continued in a noninterleaved manner. According to a variant embodiment, if the purpose is solely the non-real-time viewing of the program, without it being intended that recording should be permanent, writing is continued by overwriting the content of the previously read blocks.

According to a variant embodiment, if a recording is to be kept, then the corresponding interleaved blocks are rewritten sequentially in such a way as to deinterleave these blocks. Thus, during subsequent reading, the read head will not need to perform jumps due to the interleaving.

Of course, the invention is not limited to the exemplary embodiment given. For example, other types of disk may be used. It will be sufficient to adapt the corresponding interfaces. Consideration will in particular be given to hard disks having characteristics other than that presented hereinabove, rerecordable magneto-optical disks or other data storage media.

It should be noted that the invention applies also in the case where the audio and video data are coded differently, in particular in the case where the PES packets are contained in a program-type stream ('Program Stream') according to the MPEG standard, or the audio and video data are contained in different structures from those of the PES packets.

Moreover, although certain elements of the embodiment are presented in a distinct structural form, it is obvious to the person skilled in the art that their implementation within a single physical circuit does not depart from the scope of the invention. Likewise, the software rather than hardware implementation, or vice versa, of one or more elements does not depart from the scope of the invention: the FIFO-type memories may for example be emulated by using a conventional-addressing memory, with software management of address pointers.

It will also be noted that the data to be stored may originate from some means of transmission other than that indicated in the exemplary embodiment. In particular, certain data may travel via modem.

According to the exemplary embodiment described hereinabove, the areas of the hard disk which are reserved for each of the two file systems are fixed. According to a variant embodiment, the sizes of these areas are dynamically adapted to the requirements. Thus, there is provided a first area of system data for the 'block' file system, a second area of system data for the 'stream' file system, then a single area of blocks of the 'stream' type. The management of the 'stream' file system is performed as previously. The management of the 'block' file system is performed as follows: when a file of this type has to be recorded, the 'block' file system reserves the minimum of large-size blocks necessary, and fragments these large-size blocks (256 sectors according to the present example) into small-size blocks (four sectors). The table of bits of the nodes and the table of bits of areas of the 'block' file system manage these fragments of blocks as if they were small-size blocks.

Claims

1. A process for recording a digital video and audio data stream characterized in that, recording being carried out on a medium (201) organized in the form of logic blocks in series and comprising a recording and reading head, said process comprises the steps:
   - of recording data in one block out of two starting from a first block,
   - following the triggering of the reading of the data, alternately of reading a previously recorded block and of continuing the recording in the block following the block read.

2. The process as claimed in claim 1, characterized in that when the set of blocks recorded before the triggering of reading have been read, recording is continued in contiguous blocks in a non-interlaced manner.

3. The process as claimed in claim 1, characterized in that when the set of blocks recorded before the triggering of reading have been read, recording is continued in a loop in the blocks previously read.

4. The process as claimed in one of claims 1 or 2, characterized in that when the set of blocks recorded before the triggering of reading have been read, said blocks are read, then rewritten in a non-interlaced manner.

5. The process as claimed in one of the preceding claims, characterized in that the recording of data is performed in a group of N contiguous blocks (N > 1) out of two instead of a single block out of two.

6. The process as claimed in one of the preceding claims, characterized in that it furthermore comprises the additional step of detecting sequences of free blocks on the medium and of applying steps of recording and of reading inside such sequences.

7. A digital television receiver comprising means (101) for receiving a digital audio and video data stream, characterized in that it comprises:
   - a recording medium (201) furnished with a recording and reading head, said medium being organized in the form of logic blocks in series;
   - a control circuit (107) for managing the writing and the reading of blocks of the recording medium (201);
   - an interfacing circuit (202 to 214) for interfacing the recording medium with said control circuit (107), said control circuit initially instructing the recording of data in one block out of two starting

from a first block and subsequently, following the triggering of the reading of the data, alternately the reading of a block previously recorded and the continuing of the recording in the block following a block read.

8. The receiver as claimed in claim 6, characterized in that the control circuit instructs the recording of data in a group of N contiguous blocks (N > 1) out of two instead of a single block out of two.

Abstract

Process for the simultaneous recording and reading of a digital audio and video data stream, and receiver for implementing the process

The invention concerns a method for recording of digital video and audio dataflow characterized in that, the recording is performed on a medium (201) organized in the form of logic blocks in series and comprising a recording and reading head.

The method comprises steps which consist in:

- recording data in one block out of two starting from a first block;
- following the triggering of data reading, alternately reading a previously recorded block while proceeding with the recording while proceeding with the recording in the block coming after the read block.

The invention also concerns a digital television receiver set using said method.

Figure 9b.

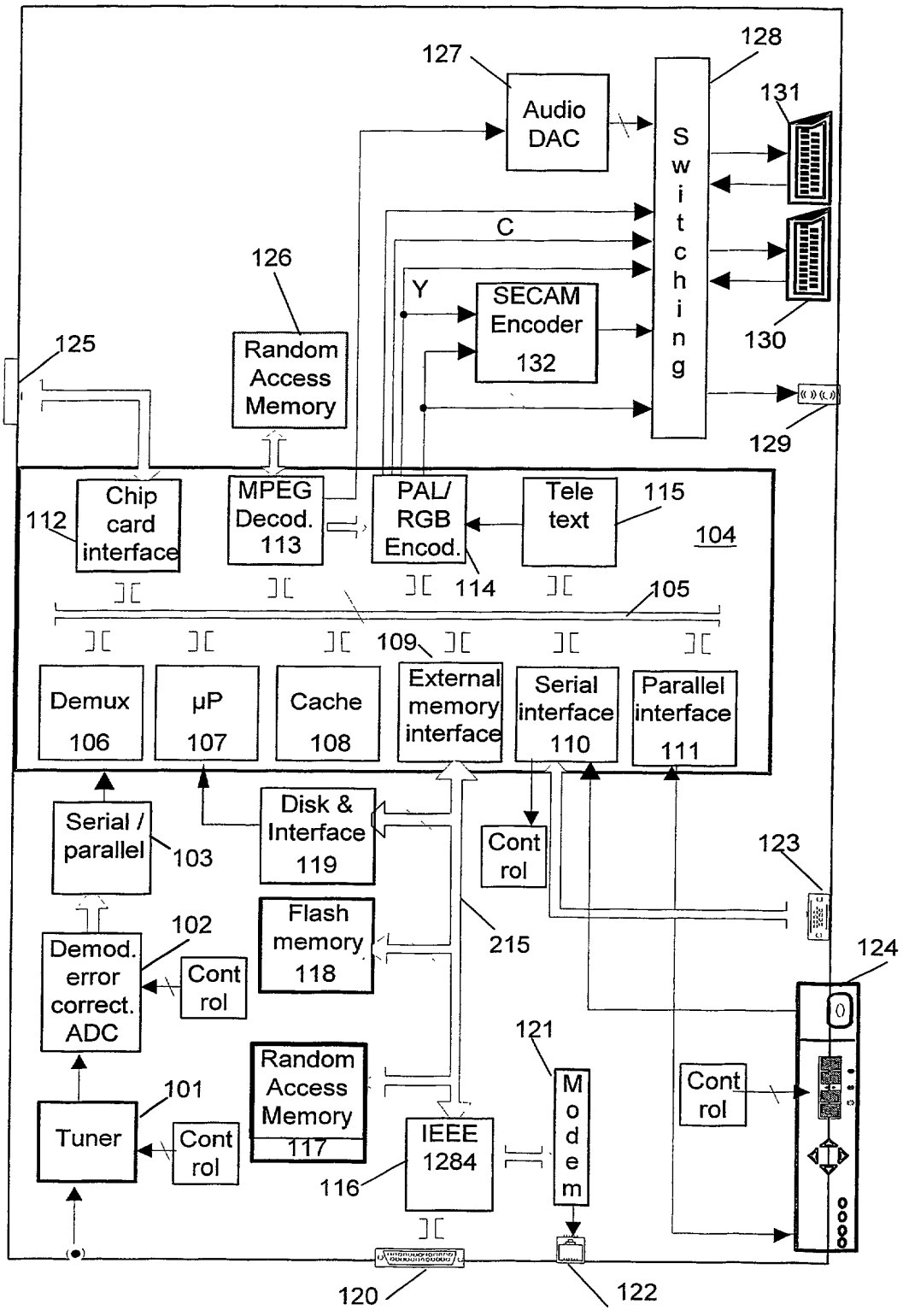

127
Audio DAC
128
Switching
131
130
129
C
Y
126
SECAM Encoder 132
125
Random Access Memory
112
Chip card interface
MPEG Decod. 113
PAL/ RGB Encod.
114
Tele text
115
104
105
109
Demux 106
µP 107
Cache 108
External memory interface
Serial interface 110
Parallel interface 111
Serial / parallel
103
Disk & Interface 119
Cont rol
123
102
Demod. error correct. ADC
Flash memory 118
215
124
121
Random Access Memory 117
Tuner
101
IEEE 1284
116
Modem
120
122

Fig. 1

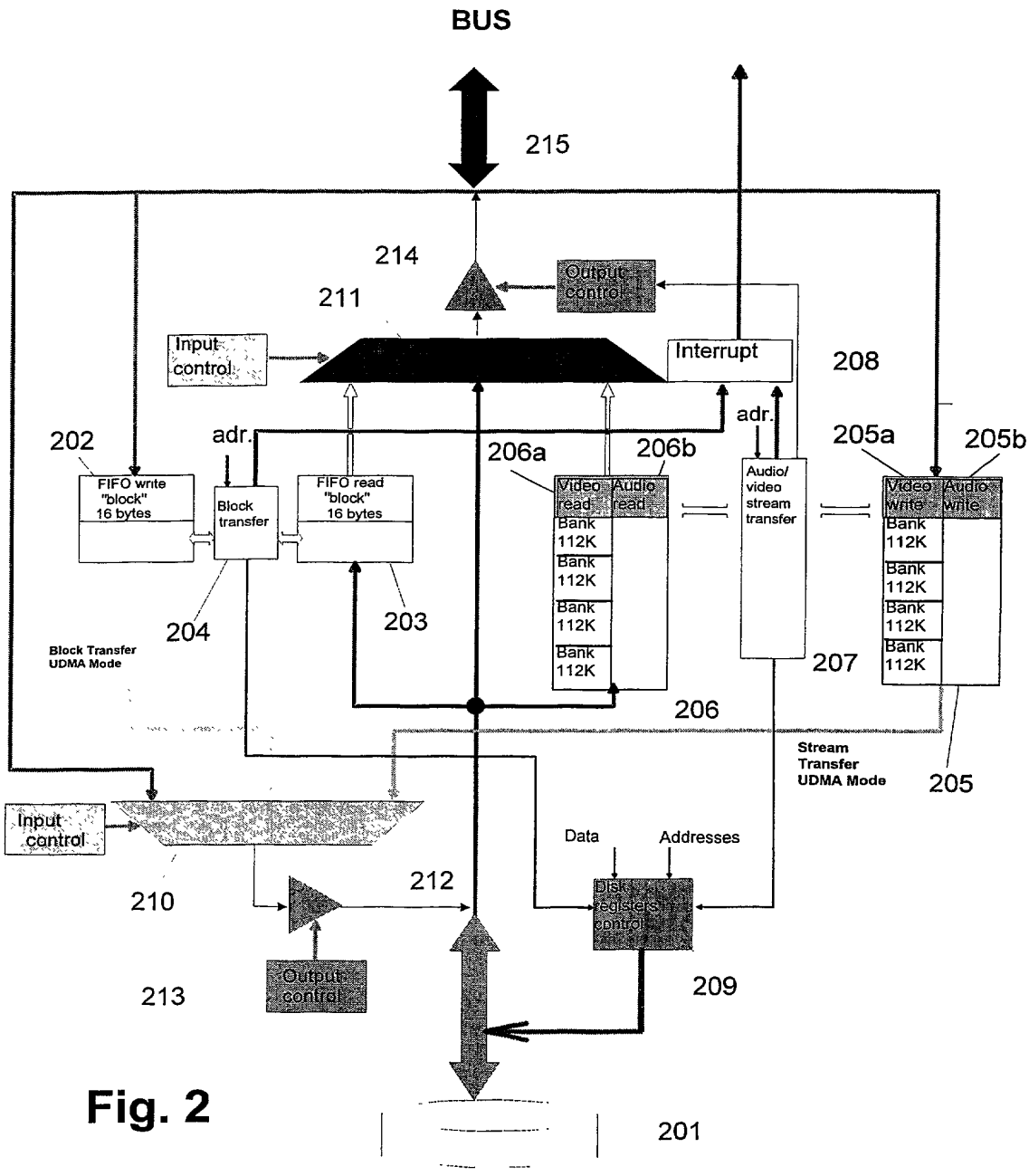

BUS
215
214
211
Output control
Input control
Interrupt
208
202
adr.
206a
206b
adr.
205a
205b
FIFO write "block" 16 bytes
Block transfer
FIFO read "block" 16 bytes
Video read
Audio read
Audio/ video stream transfer
Video write
Audio write
Bank 112K
Bank 112K
Bank 112K
Bank 112K
Bank 112K
Bank 112K
Bank 112K
Bank 112K
204
203
207
Block Transfer UDMA Mode
206
Stream Transfer UDMA Mode
205
Input control
Data
Addresses
210
212
Disk registers control
Output control
213
209
201

Fig. 2

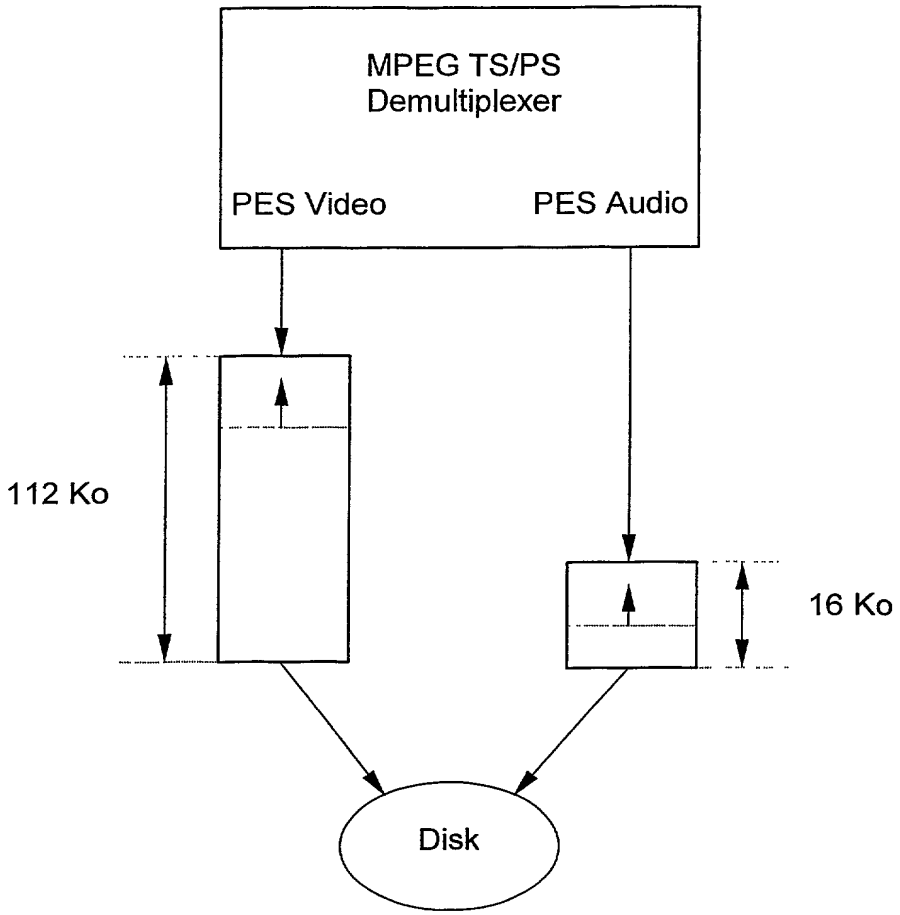

MPEG TS/PS
Demultiplexer
PES Video
PES Audio
112 Ko
16 Ko
Disk

Fig. 3

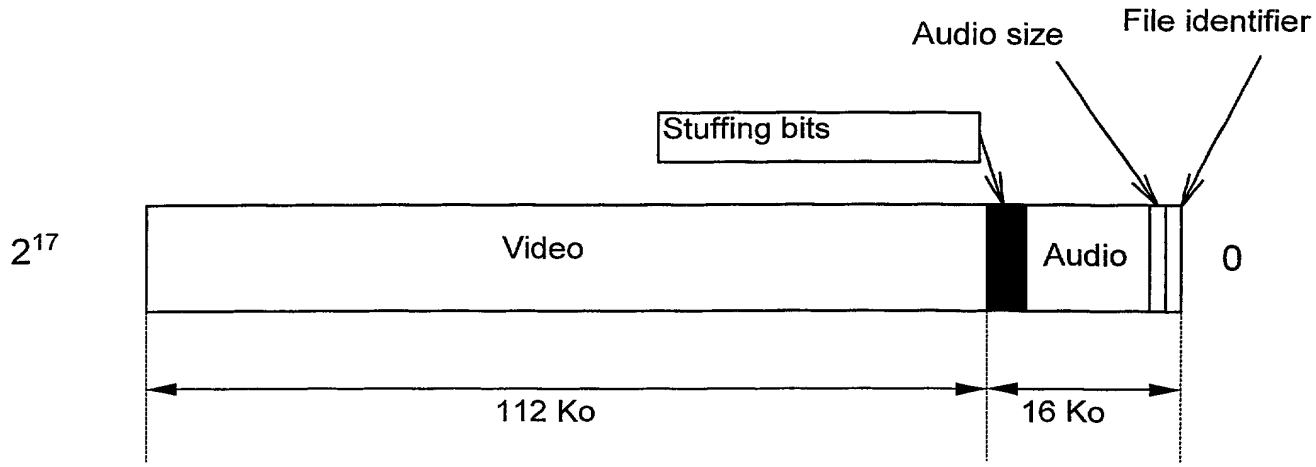

Audio size
File identifier
Stuffing bits
2^{17}
Video
Audio
0
112 Ko
16 Ko

Fig. 4

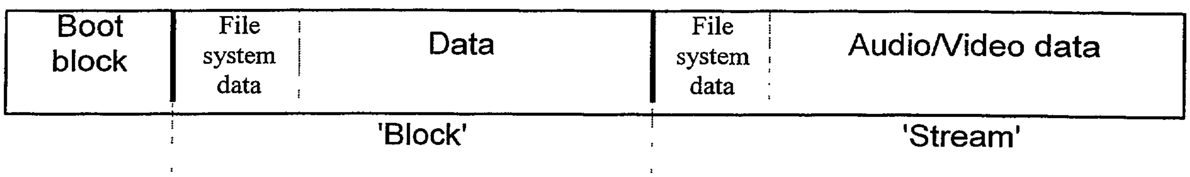

Boot block
File system data
Data
File system data
Audio/Video data
'Block'
'Stream'

Fig. 5

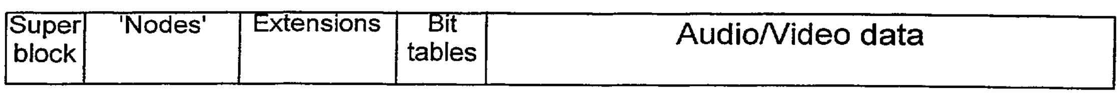
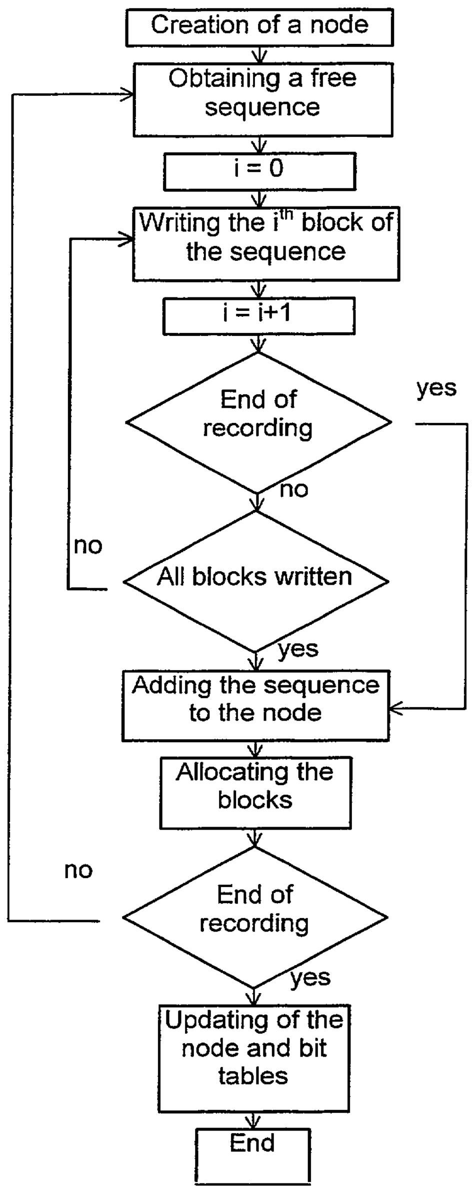

Super block
'Nodes'
Extensions
Bit tables
Audio/Video data

Fig. 6



Creation of a node
Obtaining a free sequence
i = 0
Writing the i^th block of the sequence
i = i+1
End of recording
yes
no
no
All blocks written
yes
Adding the sequence to the node
Allocating the blocks
no
End of recording
yes
Updating of the node and bit tables
End

Fig. 7

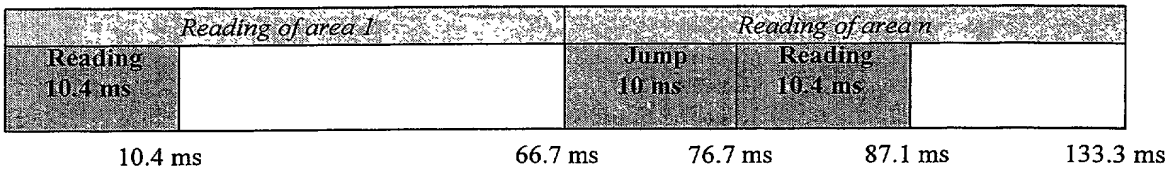


Fig. 8

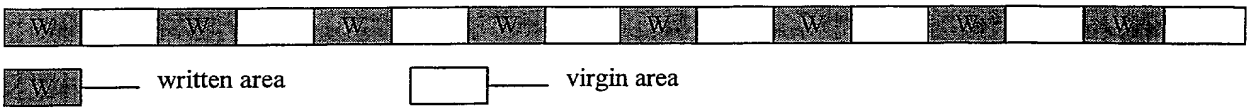


Fig. 9a

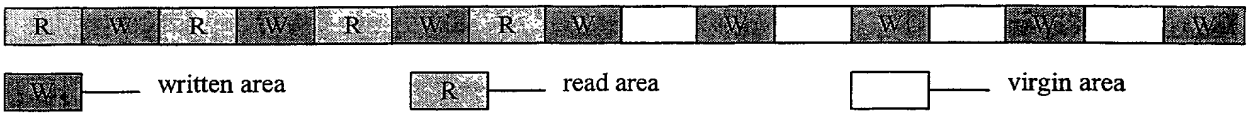


Fig. 9b

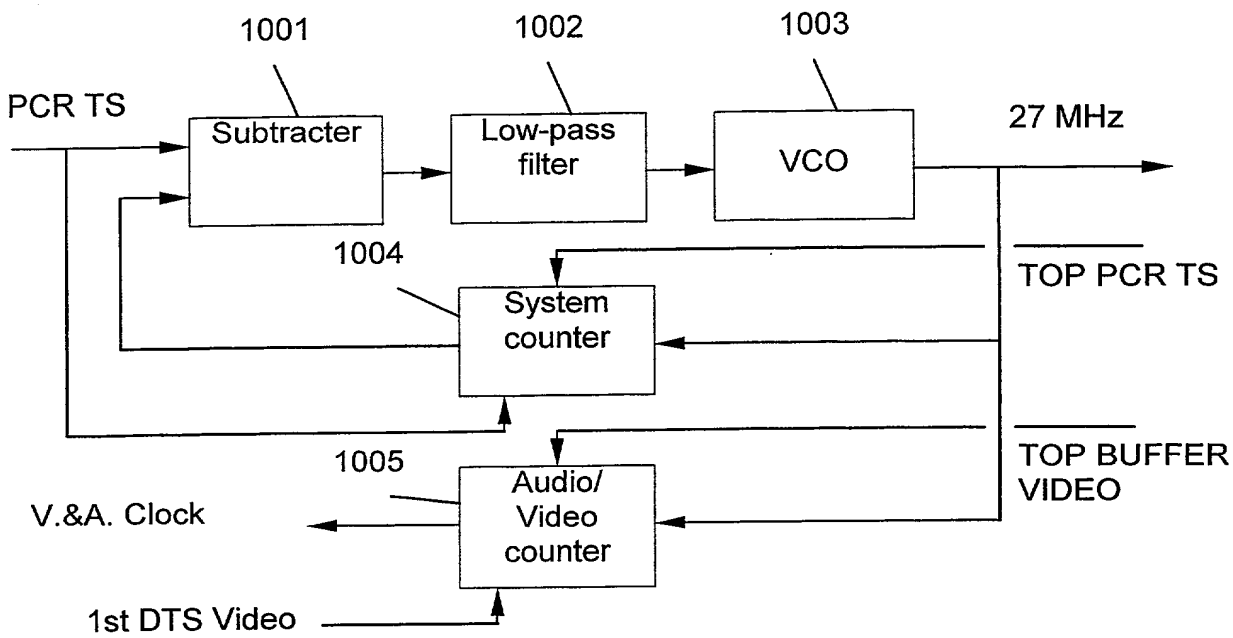


Fig. 10

DECLARATION FOR UNITED STATES PATENT APPLICATION,
POWER OF ATTORNEY, DESIGNATION OF CORRESPONDENCE ADDRESS

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"PROCESS FOR THE SIMULTANEOUS RECORDING AND READING OF A DIGITAL AUDIO AND VIDEO DATA STREAM, AND RECEIVER FOR IMPLEMENTING THE PROCESS"

the specification of which
(CHECK ONE) ( ) is attached hereto.
(XX) was filed on December 28, 1999, Application Serial. No. PCT/FR99/03298 and was amended on

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 CFR 1.56(a).

I hereby claim foreign priority benefits under 35 USC 119 of any foreign application(s) for patent, utility model, design or inventor's certificate having a filing date before that of the application(s) on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Date Filed	Yes	No
9816491	FR	December 28, 1998	xx	

I hereby claim the benefit under 35 USC 120 of any US Application(s) listed below, and, insofar as the subject matter of each of the claims of this Application is not disclosed in the prior US application in the manner provided by the first paragraph of 35 USC 112, I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 CFR 1.56(a).

Serial No.: Filed:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that wilful false statements and the like so made are punishable by fine or imprisonment, or both, under of 18 USC 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Joseph S. Tripoli (Reg. No. 26,040), Dennis H. Irlbeck (Reg. No. 26,372), Eric Herrmann (Reg. No. 29,169) and Joseph J. Laks (Reg. No. 27,914) Telephone: (609) 734-9813.

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